CLAIMS:

We claim:

1. A semiconductor device, comprising:

a semiconductor substrate having a cell array region and a peripheral circuit region;

a plurality of word line patterns placed in the cell array region of the semiconductor substrate, each word line pattern including a word line and a word line capping layer pattern;

at least one gate pattern including a gate electrode and a gate capping layer pattern located in the peripheral circuit region, the gate capping layer pattern having an etching selectivity ratio different from the word line capping layer pattern;

a plurality of gate spacers placed on side walls of the word line patterns and the at least one gate pattern;

a pad interlayer insulating layer and a bit line interlayer insulating layer sequentially stacked over a surface of the semiconductor substrate having the gate spacers, the pad interlayer insulating layer and the bit line interlayer insulating layer having approximately the same etching selectivity ratio as the gate capping layer pattern;

a cell contact hole penetrating the bit line interlayer insulating layer and the pad interlayer insulating layer in a region beween the word line patterns; and

a peripheral circuit contact hole penetrating the bit line interlayer insulating layer, the pad interlayer insulating layer, and the gate capping layer pattern to expose the gate electrode.

2. The semiconductor device of claim 1, wherein the word line and the gate electrode comprise a doped polysilicon layer.

3. The semiconductor device of claim1, wherein the word line and the gate electrode comprise a metal silicide layer.

4. The semiconductor device of claim 1, wherein the word line capping layer comprises a nitride layer.

5. The semiconductor device of claim 1, wherein the gate capping layer comprises an oxide layer.

6. The semiconductor device of claim 5, wherein the oxide layer comprises flowable oxide (FOX).

7. The semiconductor device of claim 5, wherein the oxide layer comprises spin on glass (SOG).

8. The semiconductor device of claim 1, wherein the gate spacer comprises a nitride layer.

9. The semiconductor device of claim 1, further comprising landing pads filing the cell contact hole in the region between the word line patterns.

10. A method of manufacturing a semiconductor device, comprising:

preparing a semiconductor device having a cell array region and a peripheral circuit region;

sequentially forming a gate insulating layer and a gate conductive layer on the semiconductor substrate;

forming a word line capping layer and a gate capping layer on the gate conductive layer;

patterning the word line capping layer, the gate capping layer, and the gate conductive layer to form a plurality of word line patterns in the cell array region and at least one gate pattern in the peripheral circuit region, the word line pattern including a word line and a word line capping layer pattern, the gate pattern including a gate electrode and a gate capping layer pattern;

forming gate spacers on side walls of the word line pattern and the gate pattern;

sequentially forming a pad interlayer insulating layer and a bit line interlayer insulating layer over a surface of the semiconductor substrate having the gate spacers; and

patterning the bit line interlayer insulating layer, the pad interlayer insulating layer, and the gate capping layer pattern to form a cell contact hole penetrating a region between the word line patterns and a peripheral circuit contact hole exposing the gate electrode.

11. The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the word line capping layer in the peripheral circuit region to expose the gate conductive layer;

forming the gate capping layer with an etching selectivity ratio different from the word line capping layer over a surface of the semiconductor substrate; and

planarizing the gate capping layer to expose the word line capping layer in the cell array region while retaining the gate capping layer in the peripheral circuit region.

12. The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the gate capping layer in the cell array region to expose the gate conductive layer;

forming the word line capping layer with an etching selectivity ratio different from the gate capping layer over a surface of the semiconductor substrate; and

planarizing the word line capping layer to expose the gate capping layer in the peripheral circuit region while retaining the word line capping layer in the cell array region.

13. The method of claim 10, wherein patterning the word line capping layer, the gate capping layer, and the gate conductive layer comprises:

simultaneously patterning the word line capping layer in the cell array region and the gate capping layer in the peripheral circuit region to form the word line capping layer pattern and the gate capping layer pattern, respectively; and

etching the gate conductive layer by using the word line capping layer pattern and the gate capping layer pattern as a mask.

14. The method of claim 10, wherein patterning the word line capping layer, the gate capping layer, and the gate conductive layer comprises:

patterning the word line capping layer and the gate conductive layer in the cell array region to form the word line pattern; and

patterning the gate capping layer and the gate conductive layer in the peripheral circuit region to form the gate pattern.

15. The method of claim 10, wherein patterning the word line capping layer, the gate capping layer, and the gate conductive layer comprises:

in the peripheral circuit region, patterning the gate capping layer and the gate conductive layer to form the gate pattern; and

in the cell array region, patterning the word line capping layer and the gate conductive layer to form the word line pattern.

16. The method of claim 10, wherein forming the cell contact hole comprises forming the cell contact hole using a self-align method.

17. The method of claim 11, wherein etching the word line capping layer comprises using one chosen from the group consisting of a dry-etching process, a chemical mechanical polishing process, and a wet-etching process.

18. The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the word line capping layer in the peripheral circuit region to expose the gate conductive layer;

forming the gate capping layer with an etching selectivity ratio different from the word line capping layer over a surface of the semiconductor substrate;

forming a photoresist over the gate capping layer; and

etching back the photoresist and the gate capping layer in the cell array region to expose the word line capping layer.

19. The method of claim 12, wherein etching the gate capping layer comprises using one chosen from the group consisting of a dry-etching process, a chemical mechanical polishing process, and a wet-etching process.

20. The method of claim 10, wherein forming the word line capping layer and the gate capping layer on the gate conductive layer comprises:

etching the gate capping layer in the cell array region to expose the gate conductive layer;

forming the word line capping layer with an etching selectivity ratio different from the gate capping layer over a surface of the semiconductor substrate;

forming a photoresist over the word line capping layer; and

etching back the photoresist and the word line capping layer in the peripheral circuit region to expose the gate capping layer.

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